

## 200V P-Channel Enhancement Mode MOSFET

### Description

The 4P20 is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

### General Features

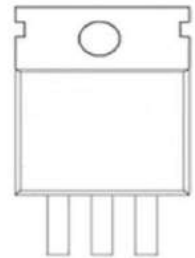
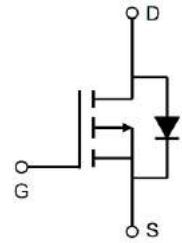
$V_{DS} = -200V, I_D = -4A$

$R_{DS(ON)} < 1.5\Omega @ V_{GS} = 10V$

### Application

Power amplifier

motor drive



### Absolute Maximum Ratings $T_C = 25^\circ C$ , unless otherwise noted

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	- 200	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current $T_C = 25^\circ C$	- 4	A
	Continuous Drain Current $T_C = 100^\circ C$	- 2.3	A
$I_{DM}$	Pulsed Drain Current <sup>a</sup>	- 14	A
$E_{AS}$	Single Pulse Avalanche Energy <sup>b</sup>	310	mJ
$I_{AR}$	Repetitive Avalanche Current <sup>a</sup>	- 3.6	A
$E_{AR}$	Repetitive Avalanche Energy <sup>a</sup>	4.2	mJ
$P_D$	Maximum Power Dissipation $T_C = 25^\circ C$	42	W
	Maximum Power Dissipation (PCB Mount) <sup>e</sup> $T_A = 25^\circ C$	2.5	W
$dV/dt$	Peak Diode Recovery $dV/dt^c$	- 5.0	V/ns
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	- 55 to + 150	$^\circ C$
$R_{thJA}$	Maximum Junction-to-Ambient	110	$^\circ C/W$
$R_{thJA}$	Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	50	$^\circ C/W$
$R_{thJC}$	Maximum Junction-to-Case (Drain)	3.0	$^\circ C/W$

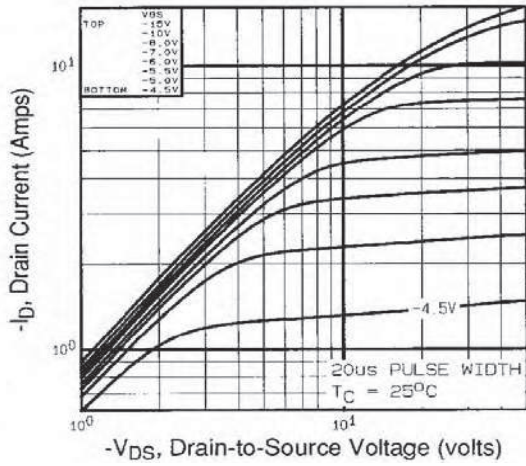
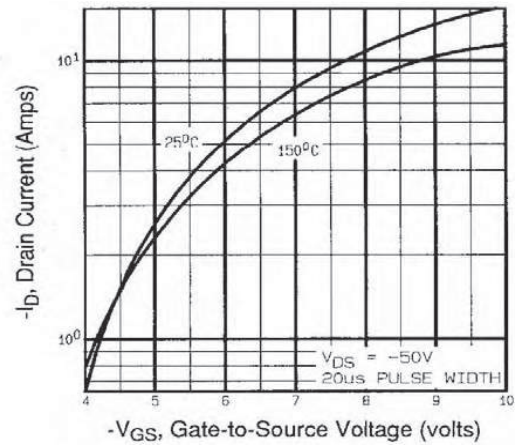
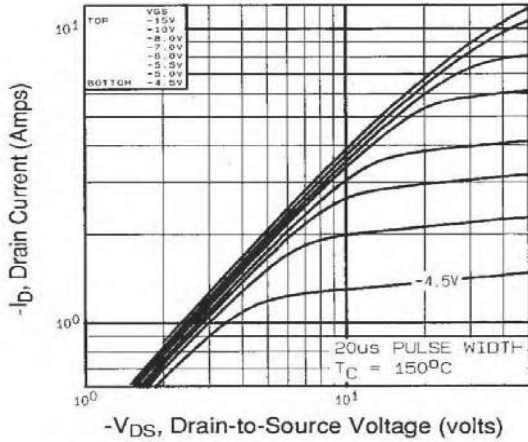
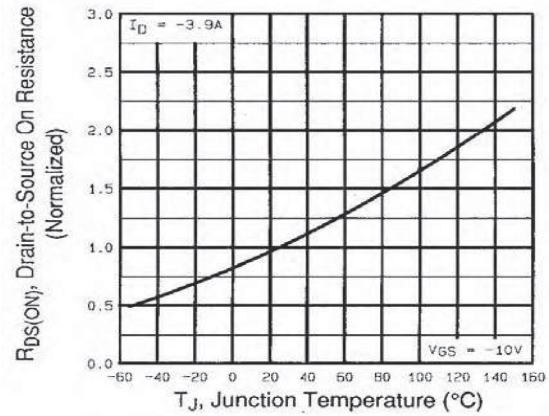
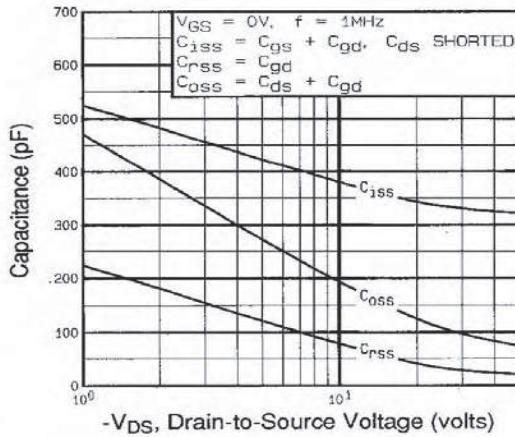
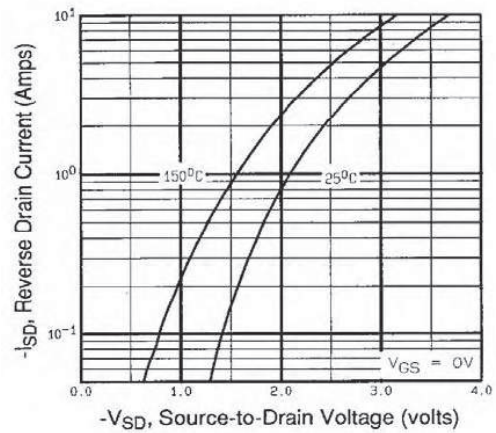
**200V P-Channel Enhancement Mode MOSFET**
**Electrical Characteristics Diagrams**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{DS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-200	-	-	V
$\Delta V_{DS}/T_J$	$V_{DS}$ Temperature Coefficient	Reference to 25 °C, $I_D = -1\text{ mA}$	-	-0.22	-	V/°C
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-2.0	-	-4.0	V
$R_{DS(on)}$	Drain-Source On-State Resistance	$V_{GS} = -10\text{ V}, I_D = -2.2\text{ A}^b$	-	-	1.5	$\Omega$
$I_{GSS}$	Gate-Source Leakage	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -200\text{ V}, V_{GS} = 0\text{ V}$	-	-	-100	$\mu\text{A}$
		$V_{DS} = -160\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ °C}$	-	-	-500	
$g_{fs}$	Forward Transconductance	$V_{DS} = -50\text{ V}, I_D = -2.2\text{ A}$	1.1	-	-	S
$C_{iss}$	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1.0\text{ MHz},$	-	340	-	pF
$C_{oss}$	Output Capacitance		-	110	-	
$C_{riss}$	Reverse Transfer Capacitance		-	33	-	
$Q_g$	Total Gate Charge	$I_D = -3.9\text{ A}, V_{DS} = -160\text{ V}, V_{GS} = -10\text{ V}$	-	-	20	nC
$Q_{gs}$	Gate-Source Charge		-	-	3.3	
$Q_{gd}$	Gate-Drain Charge		-	-	11	
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -100\text{ V}, I_D = -3.9\text{ A}, R_G = 18\ \Omega, R_D = 24\ \Omega, \text{ see fig. } 10^b$	-	8.8	-	ns
$t_r$	Rise Time		-	27	-	
$t_{d(off)}$	Turn-Off Delay Time		-	7.3	-	
$t_f$	Fall Time		-	19	-	
$I_S$	Continuous Source-Drain Diode Current	MOSFET symbol showing the integral reversep - n junction diode	-	-	-3.6	A
$I_{SM}$	Pulsed Diode Forward Current <sup>a</sup>		-	-	-14	
$V_{SD}$	Body Diode Voltage	$T_J = 25\text{ °C}, I_S = -3.6\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	-6.3	V
$t_{rr}$	Body Diode Reverse Recovery Time	$T_J = 25\text{ °C}, I_F = -3.9\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	150	300	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge		-	0.97	2.0	$\mu\text{C}$
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width  $\leq 300\ \mu\text{s}$ ; duty cycle  $\leq 2$

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**Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ C$** 

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 2 - Typical Output Characteristics,  $T_C = 150^\circ C$** 

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

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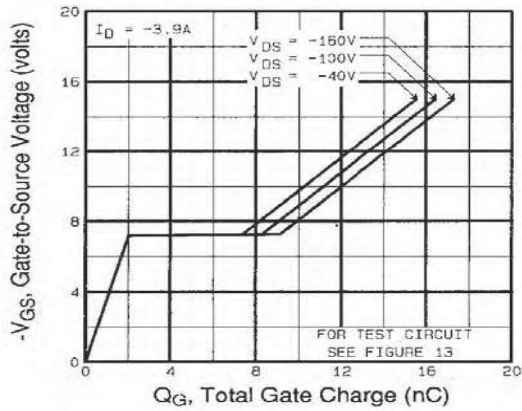


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

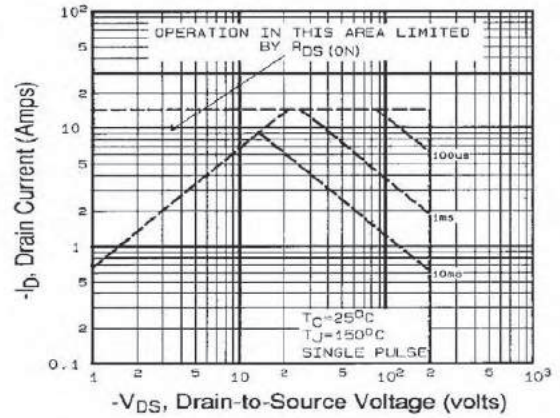


Fig. 8 - Maximum Safe Operating Area

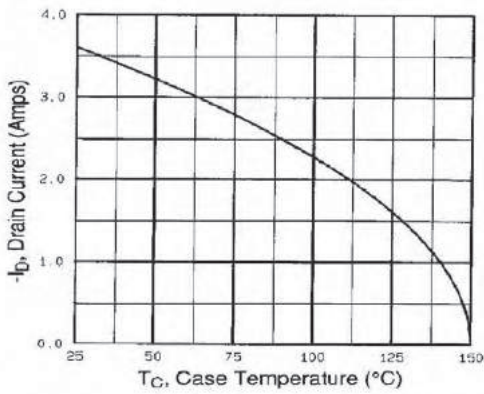


Fig. 9. Maximum Drain Current Vs. Case Temperature

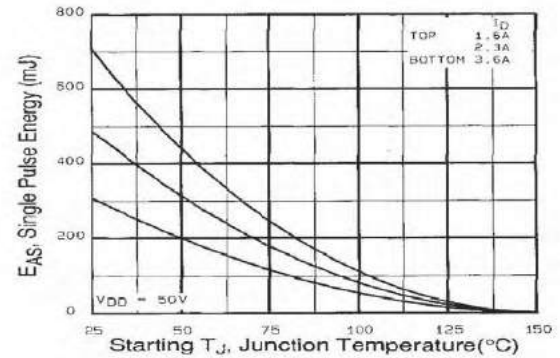


Fig. 10 - Maximum Avalanche Energy vs. Drain Current

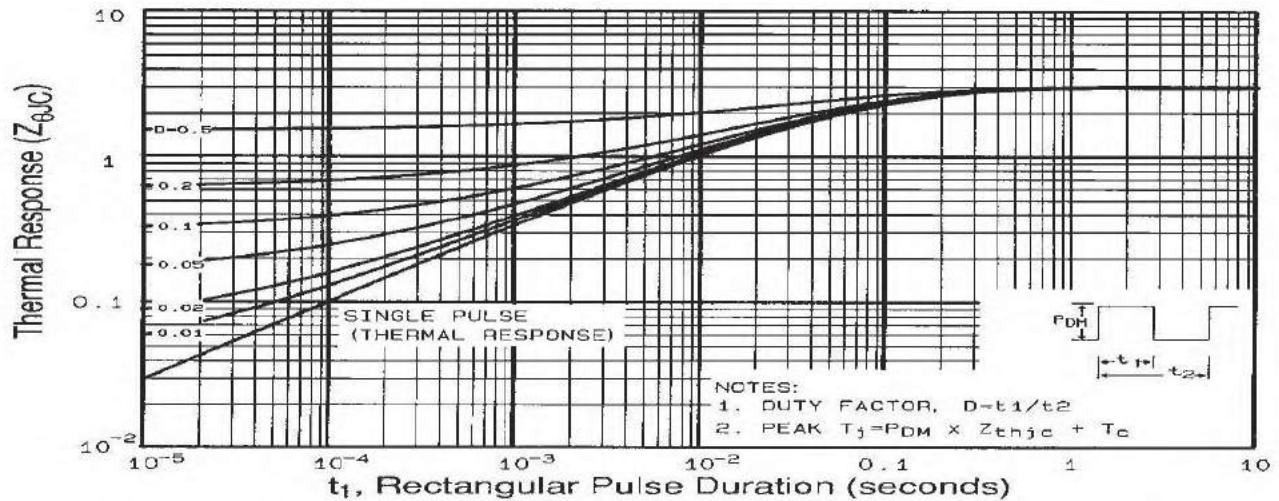
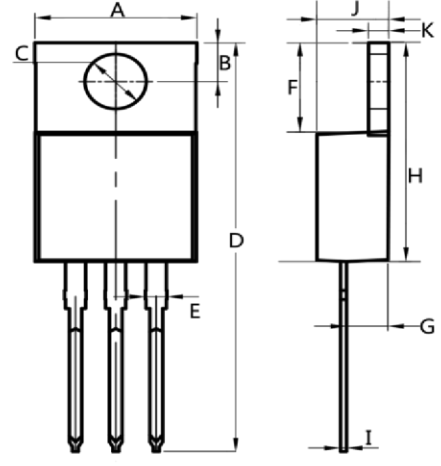


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

## 200V P-Channel Enhancement Mode MOSFET

**TO-220AB**

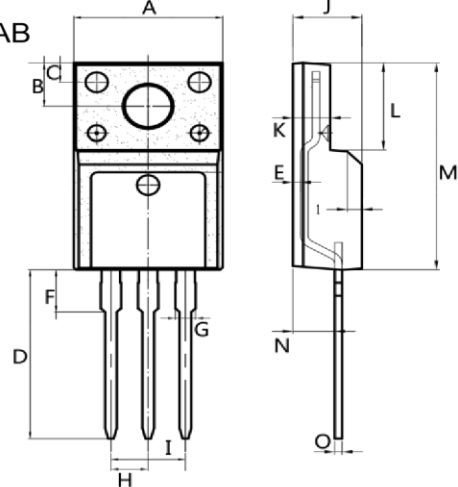


Technical drawing of the TO-220AB package showing front and side views with dimensions A through K. The front view shows a rectangular body with a circular window and three leads. The side view shows the lead profile and mounting tab.

Dim.	Min.	Max.
A	10.0	10.4
B	2.5	3.0
C	3.5	4.0
D	28.0	30.0
E	1.1	1.5
F	6.2	6.6
G	2.9	3.3
H	15.0	16.0
I	0.35	0.45
J	4.3	4.7
K	1.2	1.4

All Dimensions in millimeter

**ITO-220AB**

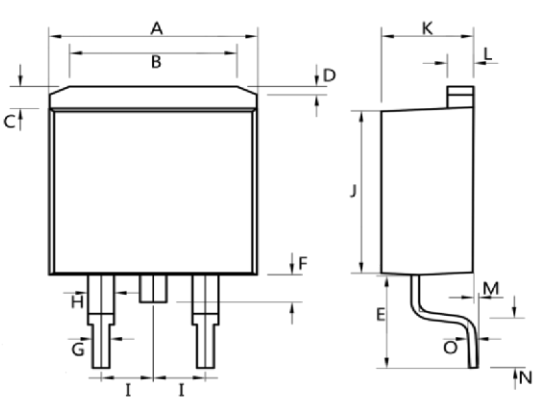


Technical drawing of the ITO-220AB package showing front and side views with dimensions A through O. The front view shows a rectangular body with a circular window and four leads. The side view shows the lead profile and mounting tab.

Dim.	Min.	Max.
A	9.9	10.3
B	2.9	3.5
C	1.15	1.45
D	12.75	13.25
E	0.55	0.75
F	3.1	3.5
G	1.25	1.45
H	Typ 2.54	
I	Typ 5.08	
J	4.55	4.75
K	2.4	2.7
L	6.35	6.75
M	15.0	16.0
N	2.75	3.15
O	0.45	0.60

All Dimensions in millimeter

**TO-263**



Technical drawing of the TO-263 package showing front and side views with dimensions A through O. The front view shows a rectangular body with a circular window and two leads. The side view shows the lead profile and mounting tab.

Dim.	Min.	Max.
A	10.0	10.5
B	7.25	7.75
C	1.3	1.5
D	0.55	0.75
E	5.0	6.0
F	1.4	1.6
G	0.75	0.95
H	1.15	1.35
I	Typ 2.54	
J	8.4	8.6
K	4.4	4.6
L	1.25	1.45
M	0.02	0.1
N	2.4	2.8
O	0.35	0.45

All Dimensions in millimeter